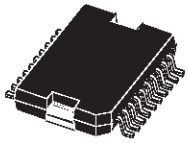
L9230

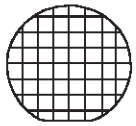
SPI CONTROLLED H-BRIDGE

PRELIMINARY DATA

- OPERATING SUPPLY VOLTAGE 5V TO 28V
- TYPICAL R_{DSon} = 150 mΩ FOR EACH OUTPUT TRANSISTOR (AT 25°C)
- CONTINOUS DC LOAD CURRENT 5A (T_{case} < 100 °C)
- OUTPUT CURRENT LIMITATION AT TYP. 6.6 A± 1.1A
- SHORT CIRCUIT SHUT DOWN FOR OUTPUT CURRENTS OVER 8A
- LOGIC- INPUTS TTL/CMOS-COMPATIBLE
- OPERATING-FREQUENCY UP TO 30 kHz
- OVER TEMPERATURE PROTECTION
- SHORT CIRCUIT PROTECTION
- UNDERVOLTAGE DISABLE FUNCTION
- DIAGNOSTIC BY SPI OR STATUS-FLAG (CONFIGURABLE)
- ENABLE AND DISABLE INPUT
- SO20 POWER PACKAGE



PowerSO20



BARE-DIE

ORDERING NUMBERS:

L9230 **L9230-DIE1**

DESCRIPTION

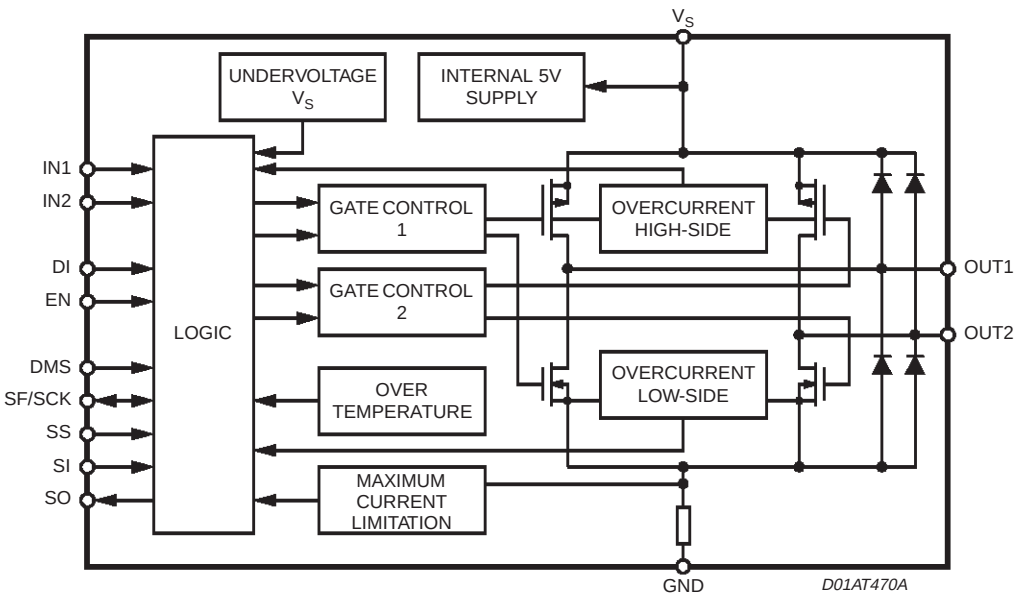
The L9230 is an SPI controlled H-Bridge, designed for the control of DC and stepper motors in safety critical applications and under extreme environmental conditions.

The H-Bridge is protected against over temperature and short circuits and has an under voltage lockout for all the supply voltages "V_S" (Main DC power supply). All malfunctions cause the output stages to go tristate.

The H-Bridge contains integrated free-wheel diodes. In case of free-wheeling condition, the lowside transistor is switched on in parallel of its diode to reduce the current injected into the substrate.

Switching in parallel is only allowed, if the voltage-level of the according output-stage is below the ground-level.In this case it must be ensured, that the upper transistor is switched off.

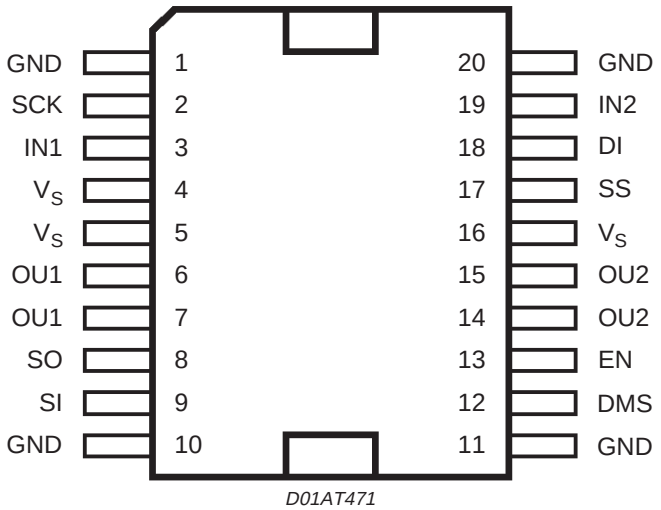
BLOCK DIAGRAM



PIN FUNCTION

N°	Pin	Description
1	GND	Ground
2	SCK/SF	SPI-Clock/Status-flag
3	IN1	Input 1
4	V_S	Supply voltage
5	V_S	Supply voltage
6	OU1	Output 1
7	OU1	Output 1
8	SO	serial out
9	SI	serial in
10	GND	Ground
11	GND	Ground
12	DMS	Diagnostic-Mode selection (+ Supply Voltage for SPI-Interface)
13	EN	Enable
14	OU2	Output 2
15	OU2	Output 2
16	V_S	Supply voltage
17	SS	Slave select
18	DI	Disable
19	IN2	Input 2
20	GND	Ground

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

The integrated circuit must not be destroyed by use at the limit values.
Each limit value can be used, as long as no other limit is violated.
Voltage reference point: All values are, if not otherwise stated, relative to ground.
Direction of current flow: Current flow into a pin is positive.
Rise-, fall- and delaytimes: If not otherwise stated, all rise times are between 10% and 90%, fall times between 90% and 10% and delay times at 50% of the relevant steps.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply voltage	static destruction proof	-1		40	V
		dynamic destruction proof t <0.5s (single pulse, Tj < 85°C)	-2		40	V
V_{LI}	Logic inputs IN1, IN2, DI, EN, SS, SI, SCK,DMS		-0.5		7	V
V_{LO}	Logic outputs SF, SO	R ≥ 10kΩ	-0.5		7	V

THERMAL DATA

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
T_j	Junction temperature	 dynamic t < 1 s	-40		+150 +175	°C °C
T_{stg}	Storage temperature		-55		+125	°C
T_{amb}	Ambient temperature		-40		+125	°C
$R_{th\ j\text{-}case}$	Thermal resistance junction to case				3	°C/W
T_{j_sd}	Thermal Shutdown Junction Temperature Threshold		165	175		°C

ELECTRICAL CHARACTERISTCS (T_j = -40 to +150°C; V_S = 5 to 28V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Power Supply						
V_S	Supply Voltage	Static Condition	5		28	V
		Dynamic Condition (t < 500ms)			40	V
	Undervoltage Shutdown	(at least down to 2.5V) (1)		4.7	5	V
I_S	Supply current	f = 0 kHz, I_O = 0 A f = 20kHz, I_O = 0 A			20 30	mA mA

Note: 1. For supply voltages down to 2.5V the output stagesare in tristate condition and the status flag is set to low. Below 2.5V the device operates in undefined condition

Logic inputs						
V_{IH}	Logic Input Voltage High IN1, IN2, DI, EN		2			V
V_{IL}	Logic Input Voltage Low IN1, IN2, DI, EN				1	V
V_H	Logic Input Voltage Hysteresis IN1, IN2, DI, EN		0.1		0.6	V
I_I	Logic Input Current IN1, IN2, DI	$V_I \le 1V$	-200	-125		µA
I_{EN}	Input Current EN	$V_{IEN} \ge 2V$			100	µA
t_{dt}	Detection Time EN, DI				20	µs

ELECTRICAL CHARACTERISTCS (T_j = -40 to +150°C; V_S = 5 to 28V) (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Power Outputs (OUT1, OUT2)						
R_S	Switch on Resistance	R_{OUT-Vs}, $R_{OUT-GND}$, V_S > 5 V			250	mΩ
	Current Limitation	Peak value controlled inductive load L = 0,8 to 5 mH ressistive load R = 0,8 to 1.8 Ω				
$\|I_{OU}\|_{max}$ $\|I_{OU}\|_{max}$	Switch-off Current	-40 °C < T_j < 165 °C T_j < 175 °C	5.5	6.6 2.5	7.7	A A
t_a	Switch-off time		12	17	22	µs
t_b	Blanking time		8	11.5	15	µs
t_a/t_b	Tracking		1.4	1.5	1.6	
$\|I_{OUK}\|$	Short circuit detection current		8		20	A
t	Reactivation time after internal shut down	Overcurrent- or overtemperature shut down to reactivation of the output stage			1	ms
I_L	Leakage Current	Output stage switched off			1	mA
V_{FD}	Free-wheel diode forward voltage	I_O = 3A			2	V
t_{rr}	Free-wheel diode reverse recovery time				100	ns
I_{SF}	Output„high“ (SF not set)	V_{SF} = 5V			20	µA
I_{SF}	Output„low“ (SF set)	V_{SF} = 1V	300			µA
		V_{SF} = 0.5V	100			µA
Timing						
f	PWM Frequency	min. operating time 10µs		2	30	kHz
f_S	Switching Frequency during current limitation			5	30	kHz
t_{don}	Output ON-delay	IN1 --> OUT1 or IN2 --> OUT2		2	5	µs
t_{doff}	Output OFF-delay			2	5	µs
t_r, t_f	Output rise-, fall Time	OUT1H--> OUT1L, OUT2H--> OUT2L, IOUT = 3 A OUT1L--> OUT1H, OUT2L--> OUT2H		3	5	µs
t_{ddis}	Disable Delay Time	DIn --> OUTn, En --> OUTn			2	µs
t_{dp}	Power on Delay Time	V_S = on --> output stage active			15	ms
	Delay time for fault detection		5		15	µs
$\|\Delta I\|$	Effect of reverse current at power supply	4,5V < V_{DMS} < 5,5V - $I_{Vs} \leq$ 3A ΔI for I_{SI}, I_{SO}, I_{SS}, I_{SCK}, I_{IN1}, I_{IN2}, I_{EN},I_{DI}			100	µA

Figure 1. Output delay time

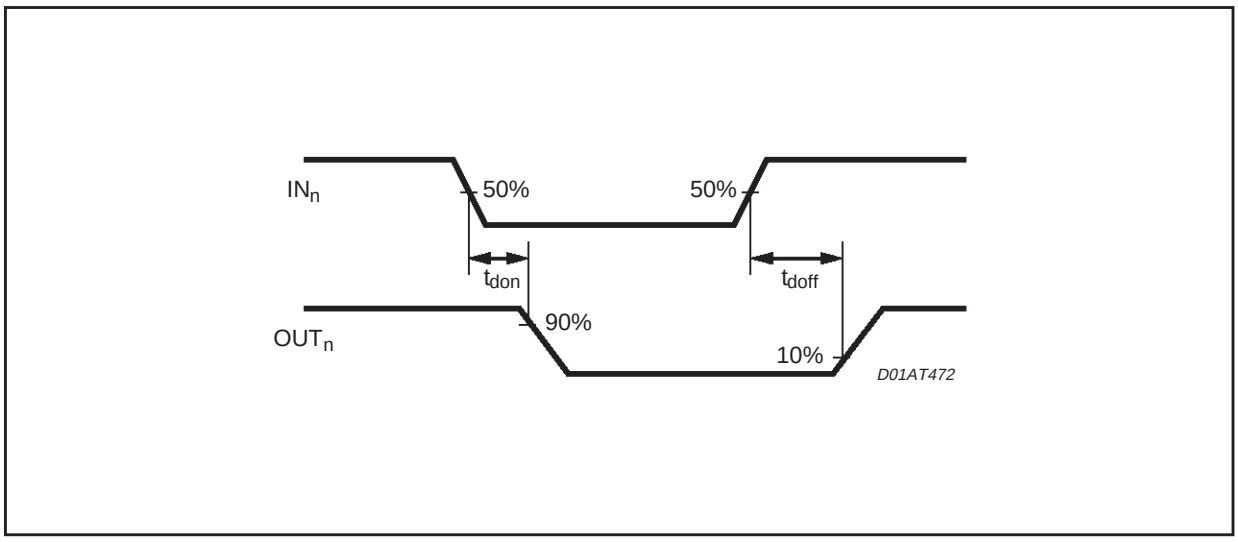


Figure 2. Disable delay time

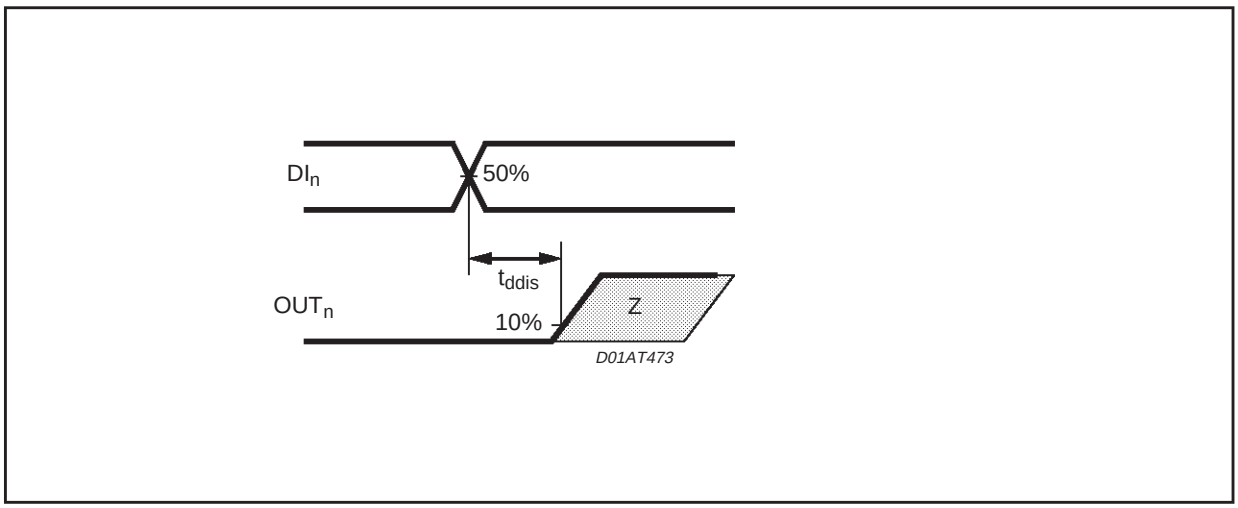


Figure 3. Output switching time

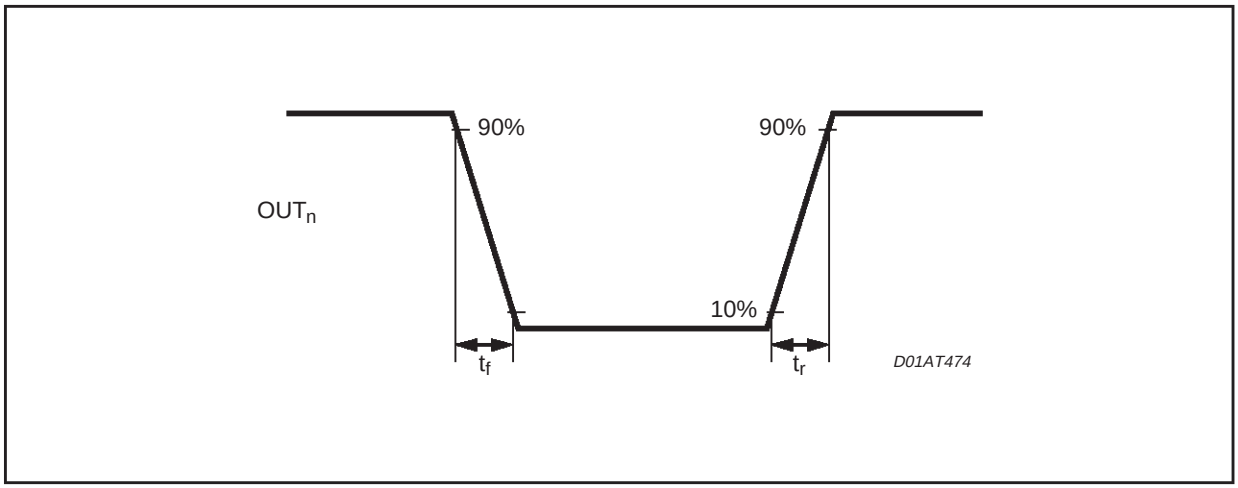


Figure 4.

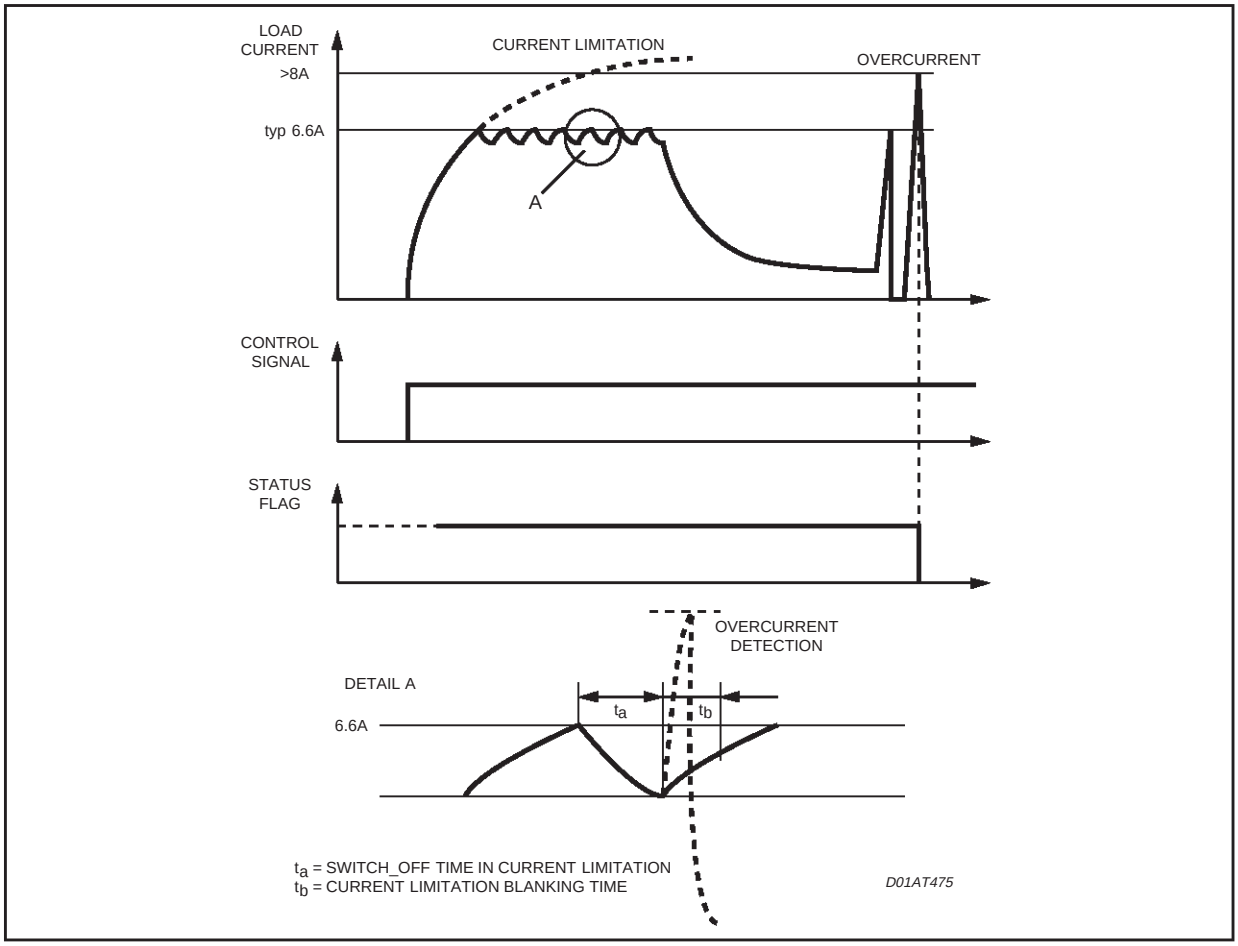
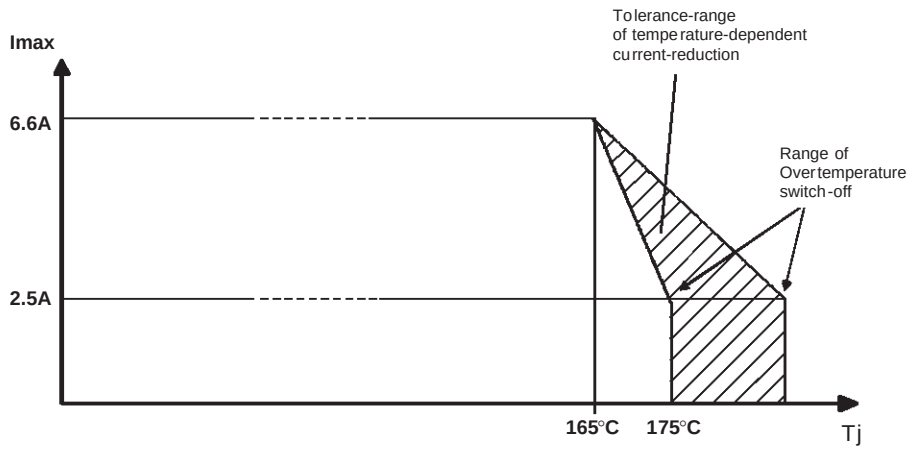


Figure 5.

Temperature-depending current-limitation

Maximum rating for junction temperature	for < 1s 175°C
Overtemperature switch-off	> 175°C
Switch-off current in case of current limitation	6,6A ± 1,1A Tj < 165°C
For 165°C < Tj < 175°C the maximum current decreases from	Imax. = 6,6A ± 1,1A to Imax. = 2,5A ± 1,1A.

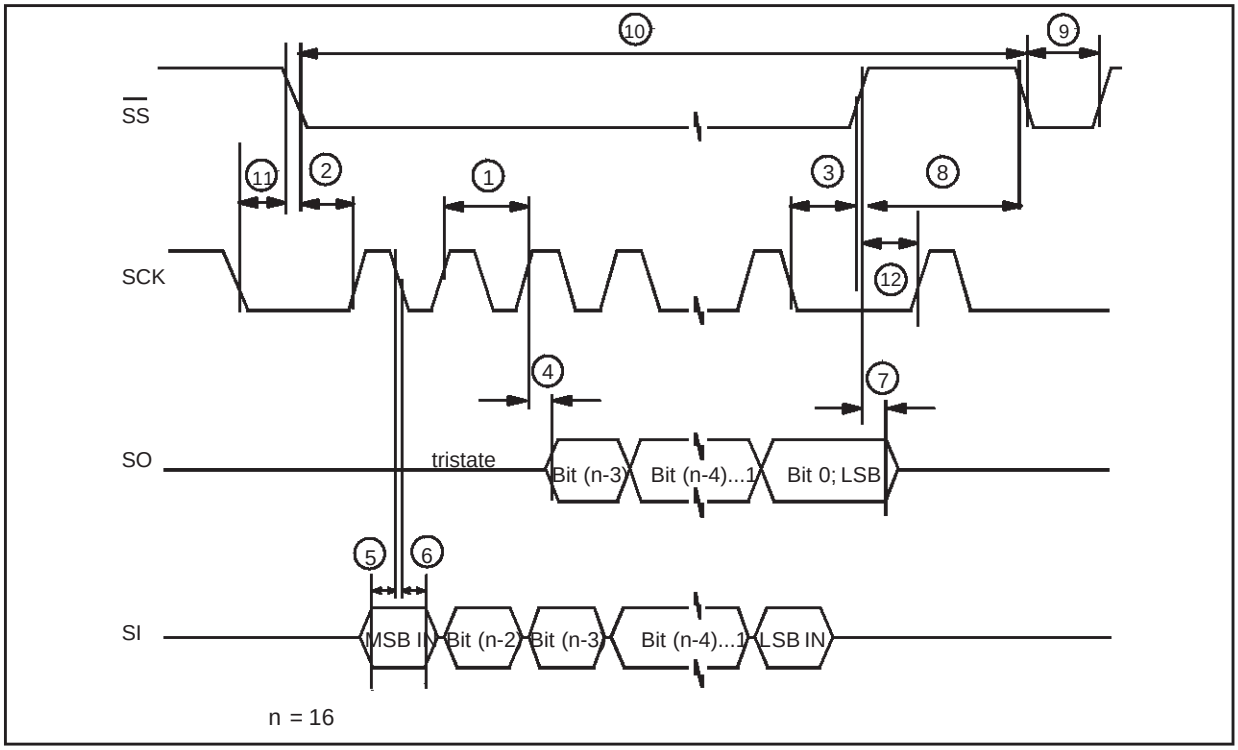


SPI INTERFACE

The timing of L9230 is defined as follows:

- The change at output (SO) is forced by the rising edge of the SCK signal.
- The input signal (SI) is taken over on the falling edge of the SCK signal.
- $\overline{SS}$ = active without any clocks at SCK is not allowed
- The data received during a writing access is taken over into the internal registers on the rising edge of the $\overline{SS}$ signal, if exactly 16 SPI clocks have been counted during $\overline{SS}$ = active.

Figure 6.



ELECTRICAL CHARACTERISTCS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Input SCK (SPI clock input 4.5V < DMS < 5.5V)						
V_{SCKL}	Low Level				1	V
V_{SCKH}	High Level		2			V
ΔV_{SCK}	Hysteresis		0.1		0.4	V
C_{SCK}	Input Capacity				10	pF
$-I_{SCK}$	Input Current	Pull up current source connected to V_S		20	50	µA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Input $\overline{SS}$ (Slave select signal)						
V_{SSL}	Low Level	L9230 is selected			1	V
V_{SSH}	High Level		2			V
ΔV_{SS}	Hysteresis		0.1		0.4	V
C_{SS}	Input Capacity				10	pF
$-I_{SS}$	Input Current	Pull up current source connected to VDD		20	50	µA
Input SI (SPI data input)						
V_{SIL}	Low Level				1	V
V_{SIH}	High Level		2			V
ΔV_{SI}	Hysteresis		0.1		0.4	V
C_{SI}	Input Capacity				10	pF
$-I_{SI}$	Input Current	Pull up current source connected to VDD		20	50	µA
Output SO (Tristate output of the L9230 (SPI output); On active reset (DI) output SO is in tristate.)						
V_{SOL}	Low Level	I_{SO} = 2mA			0.4	V
V_{SOH}	High Level	I_{SO} = -2mA	V_{VDD} - 0.75			V
C_{SO}	Capacity	Capacity of the pin in tristate			10	pF
I_{SO}	Leakage Current	In tristate	-10		10	µA
Input DMS (Supply-Input for the SPI-Inteface and Selection Pin for SPI- or SF-Mode)						
V_i	Input Voltage	SPI-Mode Status-Flag-Mode	3.5		 0.8	V V
I_c	Input Current	SPI-Mode			10	mA
Timing						
t_{cyc}	Cycle-Time (referred to master)		200			ns
t_{lead}	Enable Lead Time (referred to master)		100			ns
t_{lag}	Enable Lag Time (referred to master)		150			ns
t_V	Data Valid CL = 40pF Data Valid CL = 200pF (referred to L9230)				40 150	ns ns

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{su}	Data Setup Time (referred to master)		50			ns
t_h	Data Hold Time (referred to master)		20			ns
t_{dis}	Disable Time (referred to L9230)				100	ns
t_{dt}	Transfer Delay (referred to master)		150			ns
t_{SCKH}	Serial clock high time (referred to master)		50			µs
t_{SCKL}	Access time (referred to master)		8.35			ns
	Clock inactive before chipselect becomes valid		200			ns
	Clock inactive after chipselect becomes valid		200			ns
t_{rs}	rise-, fall time	Load on SO 50pF	20			ns
DIAGNOSTIC						
	Diagnostic Threshold (Open Load Detection DMS > 4,5V, EN < 0,8V)					
V_{OUT1} V_{OUT2}		Load is available	0.8 0.8			V V
V_{OUT1} V_{OUT2}		Load is missing	1		V_S 0.8	V V
I_{OUT2} $-I_{OUT1}$	**Diagnostic Current**	DMS > 4.5V, EN < 0.8V DMS > 4.5V, EN < 0.8V	700 1000	1000 1500	1300 2000	µA µA
	Tracking Diagnostic Current	I_{OUT1} / I_{OUT2}	1.4	1.5	1.6	
t_D	Delay Time		30		100	ms

TRUTH TABLE

Pos.	DI	EN	IN1	IN2	OUT1	OUT2	SF [3]	SPI [4] DIA_REG
1. forward	L	H	H	L	H	L	H	
2. reverse	L	H	L	H	L	H	H	
3. Free-wheeling low	L	H	L	L	L	L	H	
4. Free-wheeling high	L	H	H	H	H	H	H	
5. Disable	H	X	X	X	Z	Z	L	
6. Enable	X	L	X	X	Z	Z	L	
7. IN1 disconnected	L	H	Z	X	H	X	H	**See Page 17**
8. IN2 disconnected	L	H	X	Z	X	H	H	
9. DI disconnected	Z	X	X	X	Z	Z	L	
10. EN disconnected	X	Z	X	X	Z	Z	L	
11. Current limit. active	L	H	X	X	Z	Z	H	
12. Undervoltage [1.]	X	X	X	X	Z	Z	L	
13. Overtemperature [2.]	X	X	X	X	Z	Z	L	
14. Overcurrent [2.]	X	X	X	X	Z	Z	L	

1.) In case of undervoltage tristate and status-flag are reset automatically.

2.) Whenever overcurrent or overtemperature is detected, the fault is stored (i.e. status-flag remains low). The tristate conditions and the status-flag [3] are reset via DI or EN.

L = Low
H = High
X = High or Low
Z = High impedance
(all output stage transistors are switched off in static state. For more inform. see next page)

Overcurrent: $I_{OUT1,2}$ >8,0 A

Overtemperature: T_j >175°C

Undervoltage: V_{Vs-GND} <5.0 V (at least down to 2,5V)

3.) If Mode „Status-Flag“ is selected (see 1.5)

4.) If Mode „SPI-Diagnosis is selected (see 1.5)

Description of the state „Z“

The state „Z“ has, depending on the previous operating condition different meaning.

1. dynamical

I. e. the inductive load is current carrying and is switched off according to Pos. 5, 6, 9, 10, 11, 12, 13, or 14 of the truth table

a.) All output stage transistors are switched off.

b.) The current flow is continued via the free wheeling diodes.

c.) Free wheeling is detected by a negative voltage-level at OUn.

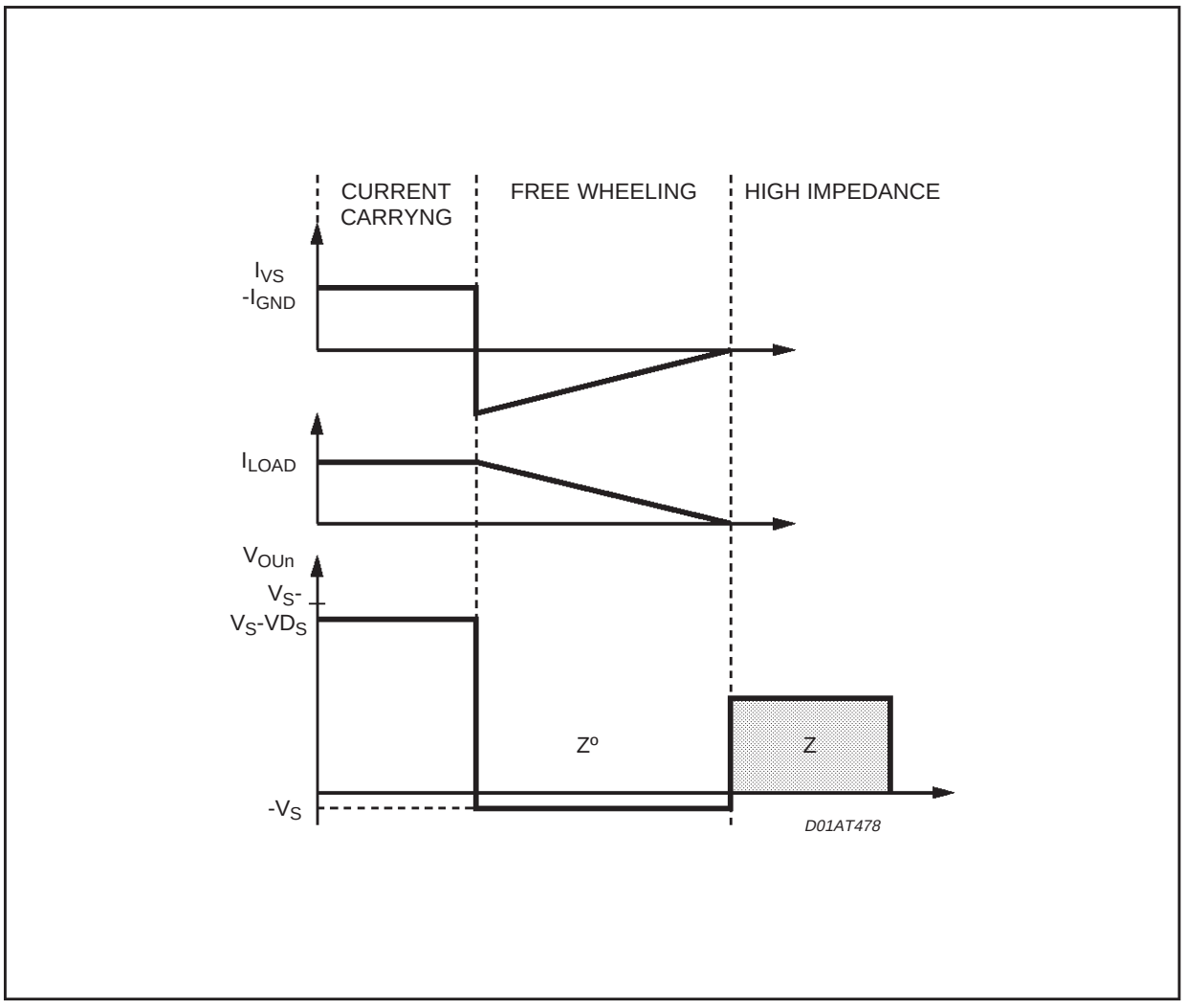
d.) Switch on of the parallel-transistor of the current carrying diode.

f.) Free wheeling is finshed, if the voltage-level on OUn is positive again.

2. statical

g.) all output-stages switched off.

Figure 7.



DIAGNOSTIC

The Diagnosis-Mode can be selected between SPI-Diagnosis and Status-Flag Diagnosis.

The choise of the Diagnosis-Mode is selected by the voltage-level on pin 12 (DMS Diagnosis Mode Selection).

DMS = GND Status-Flag

DMS = Vcc SPI-Diagnostic

For the connection of pins SI, SO, SS and SCK/SF see Fig. 10 respectively Fig. 11.

Status-Flag

The Status-Flag showes the condition „tristate".

At the following fault-cases the output-stages switches in tristate and set the status-flag from high to low.

- Short circuit of OUT1 or OUT2 against V_S or GND
- Short circuit between OUT1 and OUT2
- Overcurrent
- Overtemperature
- Undervoltage on V_S

In cause of short circuit or overcurrent, the fault will be stored.
The output stage switches in tristate and the status-flag is set from high level to low-level if the specified value is exceeded.
If the voltage level changes from high to low on DI or from low to high on EN, the output stage switches on again and the status-flag is reset to high-level.

In cause of overtemperature the fault will be stored.
The output stage switches in tristate and the status-flag is set from high level to low-level if the specified value is exceeded.
the voltage level changes from high to low on DI or from low to high on EN, the output stage switches on again and the status-flag is reset to high-level.

In cause of undervoltage on V_{Batt} the output stage switches in tristate and the status-flag is set from high level to low-level if the specified value is fallen. If the voltage has risen about the specified value again, the output stage switches on again and the status-flag is reset to high-level.

The maximum current which can flow under normal operating conditions is limited to typical $I_{max.}$ = 6,6A .
When the maximum current value is reached, the output stages are switched tristate for a fixed time.
According to the time-constant the current decreases exponentially until the next switch-on occurs.
At the end if the fixed time the output stage switches on again and the status-flag is reset to high-level.

SPI-INTERFACE

General Discription

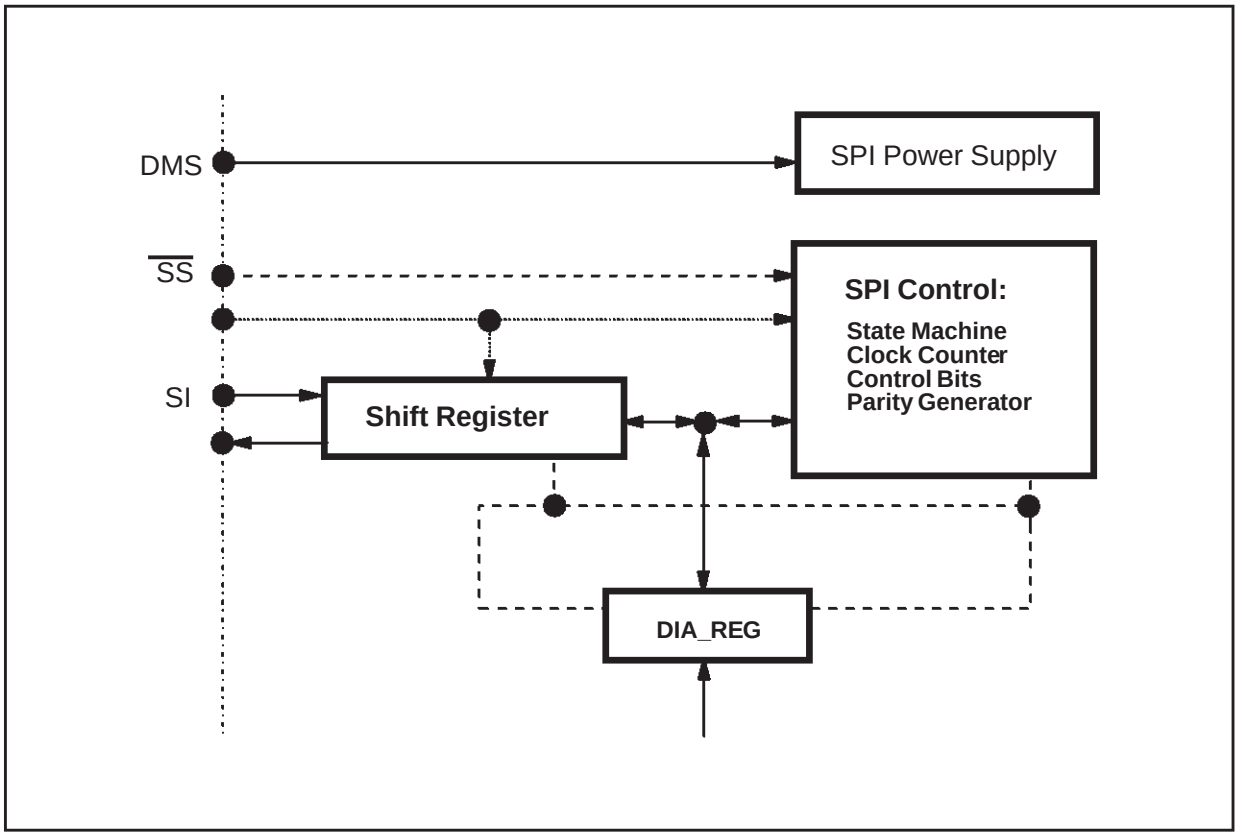
The serial SPI interface establishes a communication link between L9230 and the systems microcontroller. L9230 always operates in slave mode whereas the controller provides the master function.

The maximum baud rate is 2 MBaud (200pF).

Applying an active slave select signal at $\overline{SS}$ L9230 is selected by the SPI master. SI is the data input (Slave In), SO the data output (Slave Out). Via SCK (Serial Clock Input) the SPI clock is provided by the master.

In case of inactive slave select signal (High) the data output SO goes into tristate.

Figure 8.



Depending on the application the first two bits of an instruction may be used to estabish an extended device-addressing. This gives the opportunity to operate up to 4 Slave-devices sharing one common $\overline{SS}$ signal from the Master-Unit

Power Supply of the SPI-Interface

SPI-Logic and I/O-Pins are alternativ supplied from DMS or Vcc internal, depending on which voltage is higher.

That is why diagnosis of the EN-/DI-Pins is always possible, even in case of missing H-Bridge-power supply e.g. during „Vorlauf/Nauchlauf“.

Characteristics of the SPI Interface

1) When DMS is > 3,5V, the SPI is active, independent of the state of EN or DI and the voltage on V_S.
During active reset conditions (DMS < 3,5V) the SPI is driven into its default state.
When reset becomes inactive, the state machine enters into a waitstate for the next instruction.

2) If the slave select signal at $\overline{SS}$ is inactive (high), the state machine is forced to enter the waitstate, i.e. the state machine waits for the following instruction.

3) During active (low) state of the select signal $\overline{SS}$ the falling edge of the serial clock signal SCK will be used to latch the input data at SI. Output data at SO are driven with the rising edge of SCK. Further processing of the data according to the instruction (i.e. modification of internal registers) will be triggered by the rising edge of the $\overline{SS}$ signal. (-> See Note)

3) Chipaddress:
In order to establish the option of extended addressing the uppermost two bits of the instruction-byte (i.e the first two SI-bits of a Frame) are reserved to send a chipaddress.
To avoid a busconflict the output SO must stay high impedant during the addressing phase of a frame (i.e. until the addressbits are recognised as valid chipaddress).
This tristate behavior should be realised in any case, regardless wether the extended addressoption is used or not.
If the chipaddress does not match, the according access will be ignored and SO remains high impedant for the complete frame regardless which frametype is applied.

5) Check byte:
Simultaneously to the receipt of an SPI instruction L9230 transmitts a check byte via the output SO to the controller. This byte indicates regular or irregular operation of the SPI.
It contains an initial bitpattern and a flag indicating an invalid instruction of the previous access.

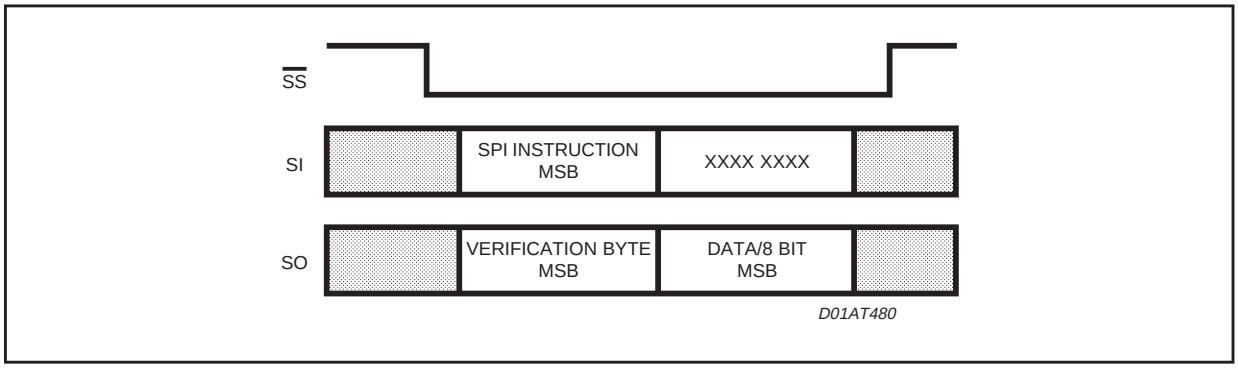
6) On the read access the databits at the SPI input SI are rejected.

7) Invalid instruction/access:
An instruction is invalid, if one of the following conditions is fulfilled:
- an unused instruction code is detected (see tables with SPI instructions).
- in case the previous transmission is not completed in terms of internal data processing.
(Violation of the minimum Access-Time.)
If an invalid instruction is detected, any modifications on registers of L9230 are not allowed.
In case an unused instruction code occured the databyte "ff_{hex}" will be transmitted after having sent the check byte.

In addition any access is invalid if the number of SPI clock pulses (falling edge) counted during active $\overline{SS}$ differs from exactly 16 clock pulses (-> See Note).

SPI Communication

Figure 9. Reading access / 8 bit



SPI Instruction

The uppermost 2 bit of the instruction byte contains the chipadress. The individual chipadress is a mask-option and must be defined in accordance to the SPI-Members sharing on SS line.

SPI Instruction-Format

MSB							
7	6	5	4	3	2	1	0
0	0	INSTR4	INSTR3	INSTR2	INSTR1	INSR0	INSW

Bit	Name	Description
7,6	CPAD1,0	Chip Adress (has to be ‘0’, ‘0’)
5-1	INSTR (4-0)	SPI instruction (encoding)
0	INSW	Don‘t care

SPI Instruction-Bytes

SPI Instruction	Encoding			Description
	bit 7,6 CPAD1,0	bit 5,4,3,2,1 INSTR(4...0)	Bit 0	
RD_IDENT	00	00000	0	read identifier
RD_VERSION	00	00001	1	read version
RD_DIA	00	00100	1	read DIA_REG
		all others		no function

Reset of the Diagnostic Register DIA_REG

On the following conditions DIA_REG is reset:

- DI high
- EN low
- With the rising edge of the SS-signal after the SPI-Instruction RD_DIA.
- When the voltage on DMS exceeds the threshold for detecting SPI-Mode. (after undervoltage condition)
- Undervoltage on V_S (< 5,0V) sets Bit 0 .... Bit 3 of DIA_REG to 0000.
- If UB rises over about the undervoltage level, the Bits of DIA_REG are restored (when V_S internal or DMS > 3,5V)

Verification byte:

MSB							
7	6	5	4	3	2	1	0
Z	Z	1	0	1	0	1	TRANS_F

Bit	Name	Description
0	TRANS_F	Bit = 1: error detected during previous transfer Bit = 0: previous transfer was recognised as valid
1		Fixed to High
2		Fixed to Low
3		Fixed to High
4		Fixed to Low
5		Fixed to High
6		send as high impedance
7		send as high impedance

Diagnostics/Encoding of Failures

Description of the SPI Registers (SPI Instructions: RD_DIA)

Register: DIA_REG							
7	6	5	4	3	2	1	0
DI	UV	OT	CurrLim	DIA21	DIA20	Dia11	DIA10

State of Reset: FFH

Access by Controller: Read only

Bit	Name	Description
0	DIA 10	Diagnosis-Bit1 of OUT1
1	DIA 11	Diagnosis-Bit2 of OUT1
2	DIA 20	Diagnosis-Bit1 of OUT2
3	DIA 21	Diagnosis-Bit2 of OUT2
4	CurrLim	is set to „0“ in case of current limitation
5	OT	is set to „0“ in case of temperature dependet current limitation
6	UV	is set to „0“ in case of overtemperature
7	DI	shows the wired-or state of the Pins EN and DI

Encoding of the Diagnostic Bits of the Output-Stages OUT1 and OUT2				
DIA21	**DIA20**	**DIA11**	**DIA10**	
-	-	0	0	Short circuit over load (SCOL)
-	-	0	1	Short circuit to battery on OUT1 (SCB1)
-	-	1	0	Short circuit to ground on OUT1 (SCG1)
-	-	1	1	No error detected on OUT1
0	0	-	-	Open load (OL)
0	1	-	-	Short circuit to battery on OUT2 (SCB2)
1	0	-	-	Short circuit to ground on OUT2 (SCG2)
1	1	-	-	No error detected on OUT2

0	0	0	0	Undervoltage on Pin UB

Description of DIA_REG Bit7

EN	DI	DIA_REG Bit7
0	0	0
0	1	0
1	0	1
1	1	0

Device Identifier

The IC's identifier is used for production test purposes and features plug & play functionality depending on the systems software release. It is made up on a device-number and a revision number each one read-only accessible via standardised instructions.
The Device number is defines once to allow indentification of different IC-Types by software.

The Revision number may be utilised to distinguish different states of hardware. The contents is divided into an upper 4 bit field reserved to define revisions correspondending to specific software releases.

The lower 4 bit field is utilised to indentify the actual maskset.

Both (SWR and MSR) will start with 0000_b and are increased by 1 every time an according modification of the hardware is introduced.

Reading the IC Identifier (SPI Instruction: RD_IDENT):

IC Identifier1 (Device ID)							
7	6	5	4	3	2	1	0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Bit	Name	Description
7...0	ID(7...0)	ID-No.: 10100001 **L9230**

Reading the IC revision number (SPI Instruction: RD_VERSION):

IC's revision number							
7	6	5	4	3	2	1	0
SWR3	SWR2	SWR1	SWR0	MSR3	MSR2	MSR1	MSR0

Bit	Name	Description
7...4	SWR(3...0)	Revision corresponding to Software release: 0Hex
3...0	MSR(3...0)	Revision corresponding to Maskset: 0Hex

Figure 10. Application example with SPI-Interface

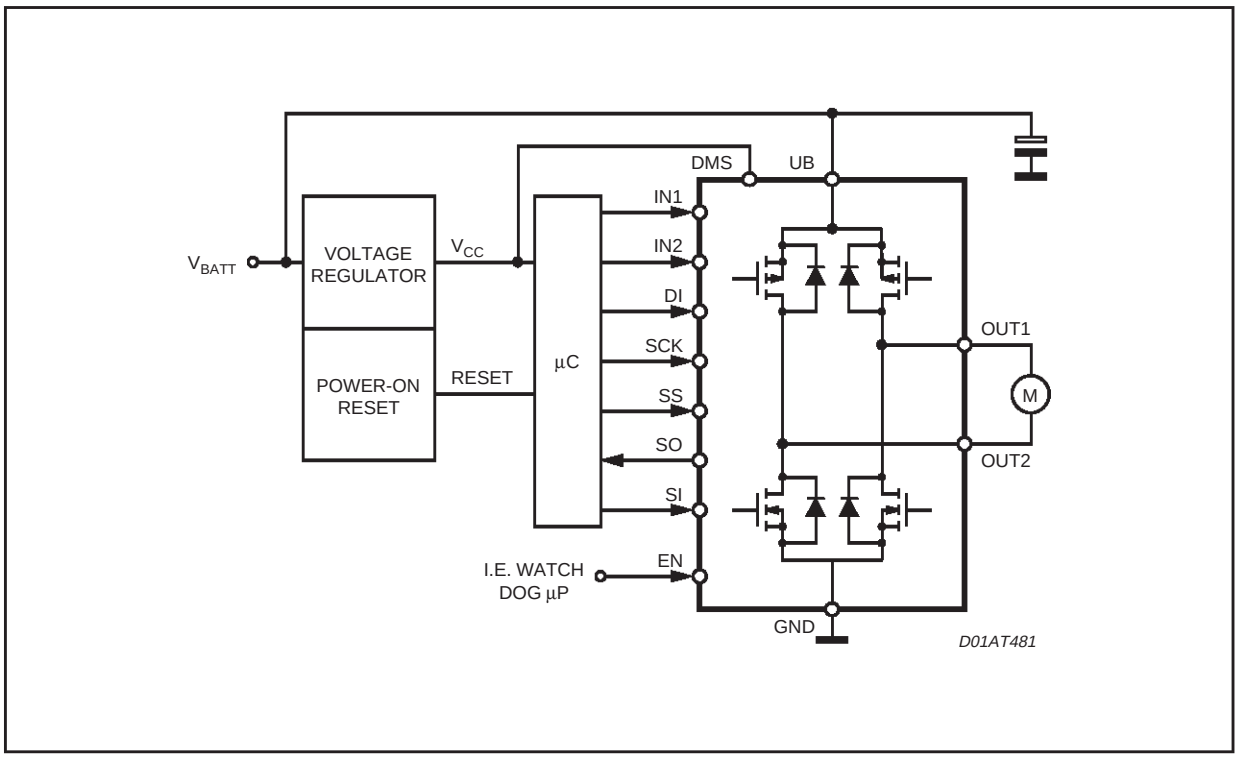


Figure 11. Application example with Status-Flag

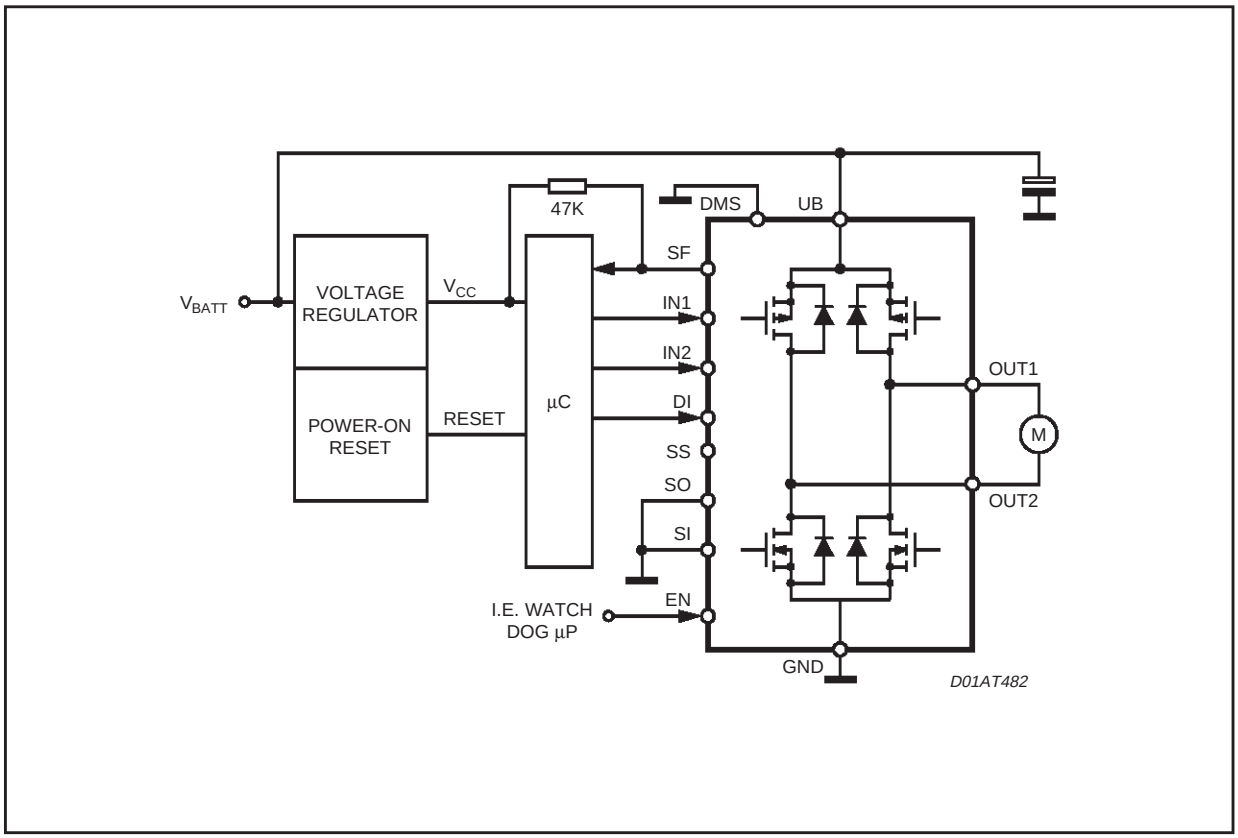
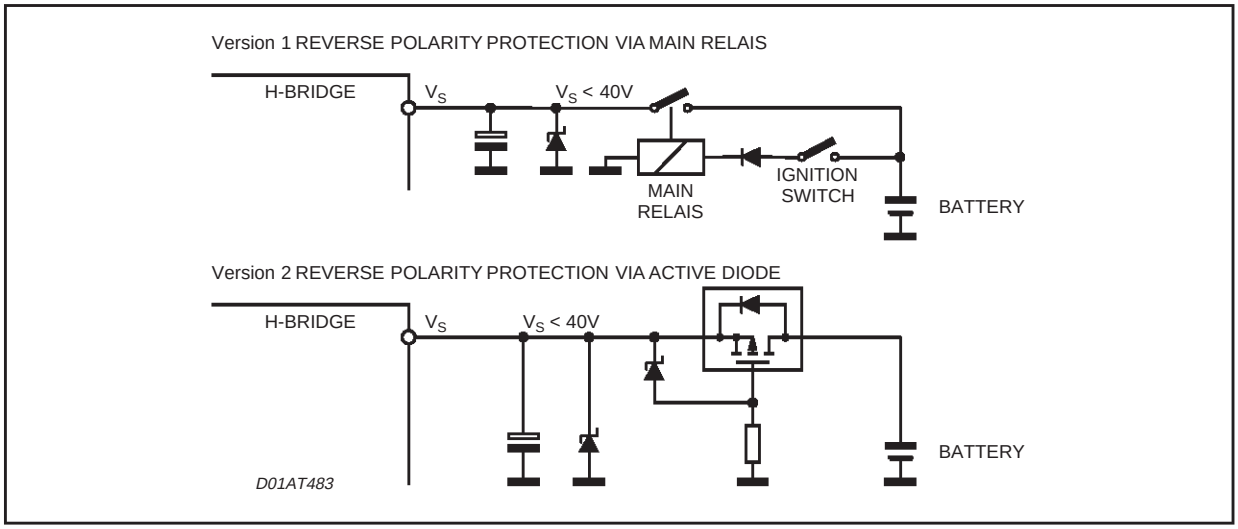


Figure 12. Application examples for Overvoltage- and Reverse-Voltage Protection



ESD-SOLIDITY

The connection pins of the IC have to be protected against Electrostatic Discharge ESD) by suitable integrated protection structures.

The integrated circuit has to meet the demand of the „Human-Body-Model“ with $V_C = \pm 4kV$

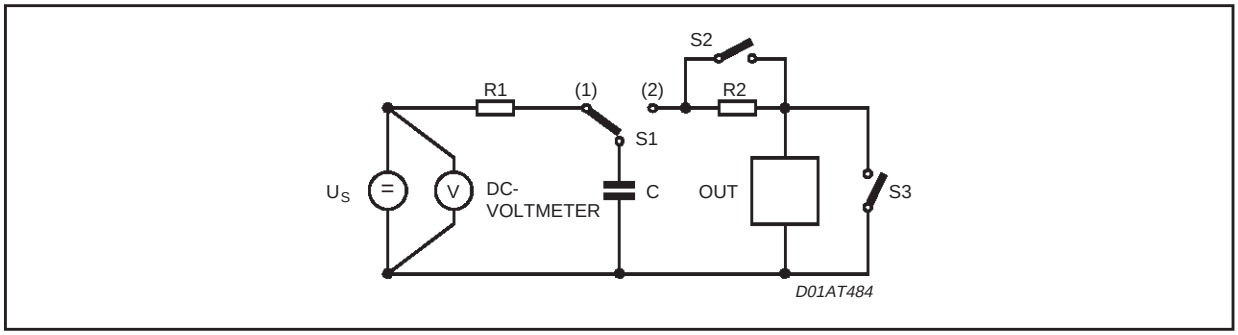
C = 100pF and R2 = 1,5kΩ (330Ω for OUT1 and OUT2).

Thereby any defect or destruction of the integrated circuit must not occur.

The protection structures realized to reach the ESD-strength have to be coordinated.

The ESD-strength has to be verified by the test circuit given as below.

Figure 13.



For the Pins 4, 5, 6, 7, 14 and 15

$U_C = \pm 4kV$

$R_1 = 100k\Omega$

$R_2 = 330\Omega$

C = 100pF

Number of pulses each pin: 18

Frequency: 1Hz

Arrangement and performance:

The requirements of MIL883D Methode 3015 have to be fulfilled.

ISO-PULSES

In the main-power-supply-system disturbance transients according to ISO 7637-1 First Edition 1990-06-01 may occur.

By means of external components (see Fig. 12) the following maximum ratings of the IC will not be exceeded.

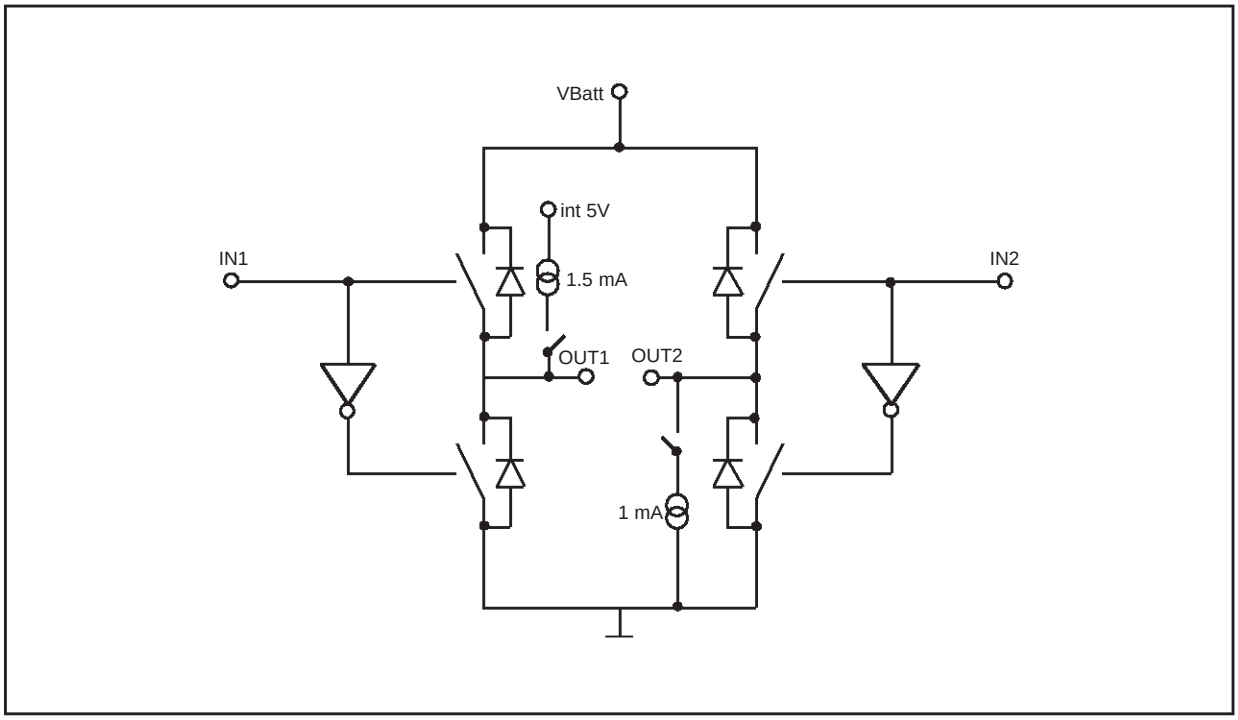
statical -1V ..... +40V

dynamical for t < 500 ms -2V ..... +40V

APPENDIX A

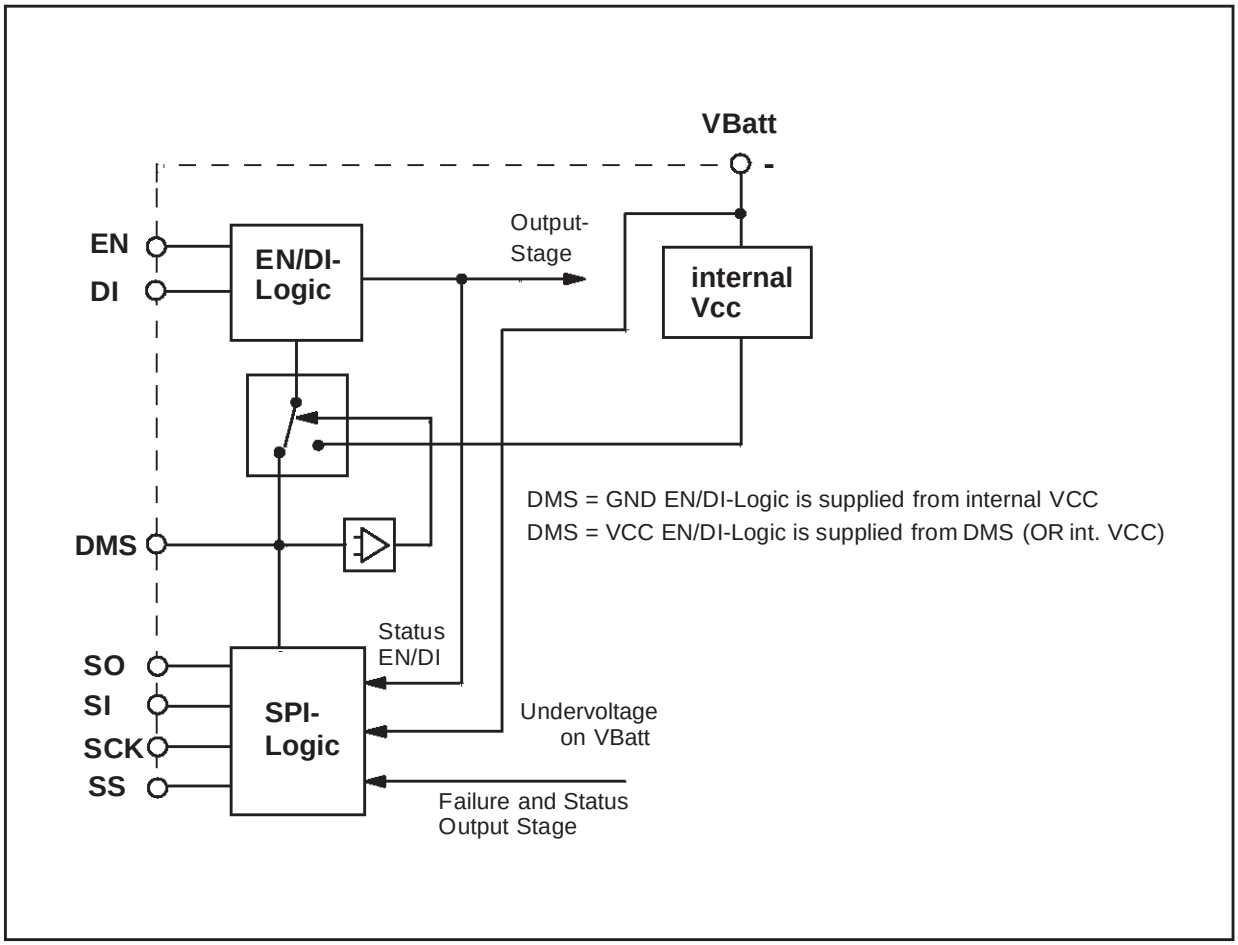
	OUT1	OUT2	
Load available	1	1	
Open Load	1	0	
SC -> GND on OUT1 with Load	0	0	SC detected on normal operation
SC -> GND on OUT2 with Load	0	0	SC detected on normal operation
SC -> UB on OUT1 with Load	1	1	SC detected on normal operation
SC -> UB on OUT2 with Load	1	1	SC detected on normal operation
SC -> GND on OUT1 Open Load	0	0	OL not detected Double Fault
SC -> GND on OUT2 Open Load	1	0	OL detected
SC -> UB on OUT1 Open Load	1	0	OL detected
SC -> UB on OUT2 Open Load	1	1	OL not detected Double Fault

Figure 14.



APPENDIX B

Figure 15. Voltage Supply of SPI-Logic and EN/DI-Logic

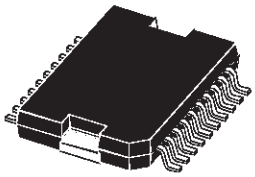


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	8° (typ.)					
S	8° (max.)					
T		10			0.394	

(1) "D and E1" do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006")
- Critical dimensions: "E", "G" and "a3".

OUTLINE AND MECHANICAL DATA

Weight: 1.9gr



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